ASICS.ws

Line Card

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Introduction

This brochure summarizes most commercial IP cores currently provided by ASICS.ws. In addition to these commercial IP cores we also provide over 32 Free IP cores that can be freely downloaded from our web site. If you can not find what you are looking for, please contact us (info@asics.ws) and we will try to find a solution for you.

I hope you find this brochure and our products helpful.

Sincerely,
Rudolf Usselmann
General Manager

Enhanced AES (Rijndael) IP Core

FIPS-197 Compliant. Encrypt and decrypt modules with 128, 192 and 256 bit keys. Various versions are available, from small area to high performance, up to 34 Gbps in 0.18u. CCM mode is also available.

http://www.asics.ws/doc/aes_brief.pdf

Enhanced Floating Point Unit

This is a fully configurable collection of Floating Point functions that are fully IEEE-754-1985 compliant and can be used to build floating point units and dedicated functions that require floating point math. Precision is fully parametrized and can be freely selected (for example: 32, 64, 80 or 128 bit).

http://www.asics.ws/doc/efpu_brief.pdf

16 Bit RISC MCU

A 16 bit true RISC Architecture Microcontroller for embedded applications that require high performance in a small form factor with ultra low power consumption. Fully configurable.

http://www.asics.ws/doc/rmcu_brief.pdf

16 Bit RISC DSP

A 16 bit true RISC Architecture Digital Signal Processor for embedded applications that require high performance in a small form factor with ultra low power consumption.

http://www.asics.ws/doc/rdsp_brief.pdf

USB 2.0 On-The-Go (LS/FS/HS)

A 'Dual-Role' USB On-The-Go IP Core that operates as both an USB peripheral or as an USB OTG host in a point-to-point communications with another USB device. This USB IP Core supports both High Speed and Full Speed transfers and automatic line speed negotiation. Includes a UTMI L2+ PHY interface. Fully USB 2.0 and USB 2.0 OTG Supplement Compliant.

http://www.asics.ws/doc/otg_brief2.pdf

USB 2.0 Device (FS/HS)

A USB 2.0 Device IP Core that provides high performance small footprint solution for quick and easy implementation of a USB Device interface. The USB 2.0 Device IP Core is fully USB 2.0 compliant.

http://www.asics.ws/doc/dev_brief.pdf

Serial ATA (1.5-3.0 Gbps) Host

The Serial ATA I/II Link and Transport Layer Core provides an interface to high-speed serial link replacements for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes Gigabit technology and 8b/10b encoding.

http://www.asics.ws/doc/sata_brief.pdf

SATA Port Multiplier

The SATA Port Multiplier allows a single SATA link layer to used with 2-15 SATA ports, expanding the number of drives for a single application enormously.

http://www.asics.ws/doc/sata_pm_brief.pdf

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http://www.asics.ws/doc/sata_device_brief.pdf

Reed Solomon Decoder

A high performance, fully configurable Reed Solomon Decoder IP Core that is intended for use in a wide range of applications requiring forward error correction. It can be targeted for both ASIC and FPGA technologies.

http://www.asics.ws/doc/rsd_brief.pdf

Reed Solomon Encoder

A high performance, fully configurable Reed Solomon Encoder IP Core that is intended for use in a wide range of applications requiring forward error correction. It can be targeted for both ASIC and FPGA technologies.

http://www.asics.ws/doc/rse_brief.pdf

I2C Master and Slave

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

SD/SDIO/MMC Host IP Core

A complete, easy to integrate and cost-effective IP core featuring SD/SDIO/MMC Host Controller Interface, for SoC/PDA applications that connect to SD/MMC memory cards and SDIO/mixed devices such as Bluetooth device. Supports 1-8 bit interface as well as CE-ATA.

http://www.asics.ws/doc/sd_mmc_brief.pdf

SD/SDIO/MMC Device IP Core

A compact low power and scalable IP core which provides a simple, firmware-friendly cost-effective Physical Link interface for memory, i/o and combo devices, such as SD-based memory cards, Mini SD, Micro SD, SDIO Bluetooth devices, SDIO GPS, MMC memory cards, MMC-RS, MMC-Mobile, CE-ATA devices etc etc.

http://www.asics.ws/doc/mmc_card_brief.pdf

http://www.asics.ws/doc/sd_card_brief.pdf

GPON FEC 2.5 Gbps

This high performance core is a full featured Forward Error Correction encoder and decoder, specially designed for high speed optical networks or any other broadband applications. It is fully compliant with the 2.5 Gbps GPON standard (G.984.3) and is available for FPGA or ASIC implementation. The FEC algorithm is based on Reed-Solomon (255,239) code and consists of an encoder and decoder module. The encoder module computes 16 parity bytes and appends them on the 239 byte information block. The decoder receives the 255 bytes codeword, locates and corrects up to 8 byte errors being introduced in the transmission channel.

http://www.asics.ws/doc/gpon_brief.pdf

SPI Flash Controller

The SPI FLASH controller provides an simple interface to serial FLASH devices, which are memory mapped in to the SoC memory space.

http://www.asics.ws/doc/spi_wb_brief.pdf

ATA-7 Target IP Core

This is a ATA-7 compliant device interface core to interface custom devices to an IDE controller. It supports ATA-7 up to UDMA 133, as well as all other modes such as PIO, MDMA and UDMA 2-6. The IP Core is targeted for SOC implementations in ASIC and FPGA.

http://www.asics.ws/doc/ata7_target_brief.pdf

ATA-7 Host IP Core

This is a ATA-7 compliant host controller core used for interfacing ATA devices like hard-disks, CD/DVD, and Compact Flash devices. This IP Core is targeted for SOC implementations in ASIC and FPGA.

http://www.asics.ws/doc/ata7_host_brief.pdf

Bus Bridges

The following bus bridges are also available:

- AHB – WISHBONE
- OPB – WISHBONE
- AVALON - WISHBONE

All ASICS World Services, LTD. IP Cores now support the following buses:

✓AHB ✓OPB ✓AVALON ✓WISHBONE ✓CUSTOM