

### USB 2.0 Device IP Core



#### INTRODUCTION

A USB 2.0 Device IP Core that provides high performance small footprint solution for quick and easy implementation of a USB Device interface.

#### FEATURES

The USB 2.0 Device IP Core is fully USB 2.0 compliant. The main features of the USB 2.0 Device IP Core are:

- USB 2.0 high performance operation
- UTMI+ L2 Interface, ULPI wrapper and FS only transceiver interface available
- Full USB peripheral support
- High Speed and Full Speed mode support
- Up to 16 endpoints
- Bulk, interrupt and isochronous transfers
- Slave and Master System Interface:
  - ✓ AHB
  - ✓ OCP
  - ✓ PLB
  - ✓ Customer specified bus interface
  - ✓ AVALON
  - ✓ OPB
  - ✓ WISHBONE
- No dedicated local memory required
- Compact and cost-effective solution for SoC

An USB 2.0 Device IP Core is ideal for applications where the target device must act as a peripheral only. It provides portable devices with a cost-effective way of conducting point-to-point communications using the USB bus.

#### ARCHITECTURE

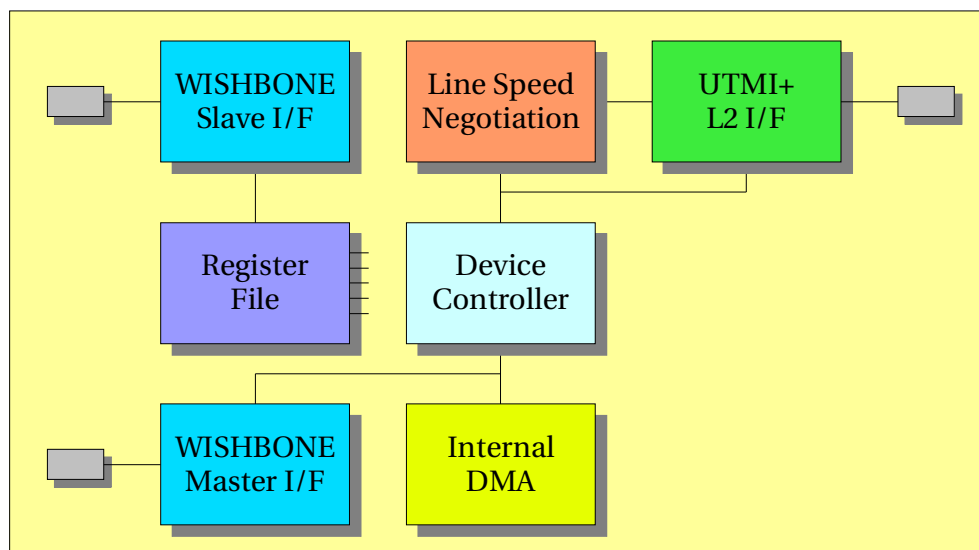
The USB 2.0 Device IP Core supports both High Speed and Full Speed operations. It will automatically perform the required negotiation to determine if it's counter part supports High Speed and fall back to Full Speed operation if it does not. The speed negotiation is supported in device and host modes.

#### UTMI+ L2 PHY Interface

The USB 2.0 Device IP Core features an industry standard UTMI+ L2 interface. Any of-the-shelf UTMI+ L2 compliant PHY or PHY IP can be used with this IP Core.

#### ULPI Interface

An optional ULPI interface is provided for interface to a ULPI compliant PHY. The ULPI interface option reduces the typical pin count of UTMI+ L2 from over 30 to just 12 interface signals.



### ARCHITECTURE (CONT.)

#### MCU Interfaces

The USB 2.0 Device IP Core features two WISHBONE interfaces:

The Slave Interface is used to access all core internal registers.

The Master Interface allows the USB 2.0 Device IP Core to share the system memory for buffering data. It is also used to store Transfer Descriptors when operating in Host Mode.

#### Buffer Memory

The USB 2.0 Device IP Core does not need dedicated buffer memory. Its WISHONE Master Interface and the internal DMA engine allow it to share the SoC's main memory for its buffers. Optionally we can also provide a WISHBONE bridge to attach standard dedicated SRAM.

### VERIFICATION

The USB 2.0 Device IP Core comes with an elaborate test bench that demonstrates the usage and programming of the USB 2.0 Device IP Core.

### SIZE AND SPEED

Sample synthesis results for an implementation with 4 endpoints.

<i>Technology</i>	<i>Gate Count</i>	<i>Operating Frequency</i>
UMC 0.18u	TBD	60 MHz PHY, TBD Mhz SoC
Xilinx Virtex II (XC2V1000-4)	1907 Slices (24% utilization )	60 MHz PHY, 160 Mhz SoC
Xilinx Spartan-3™ (XC3S1000-5)	1889 Slices (36% utilization )	60 MHz PHY, 150 Mhz SoC

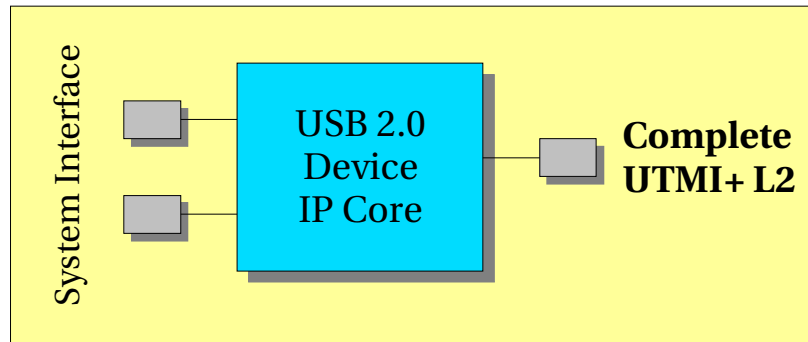
These synthesis results are provided for reference only. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

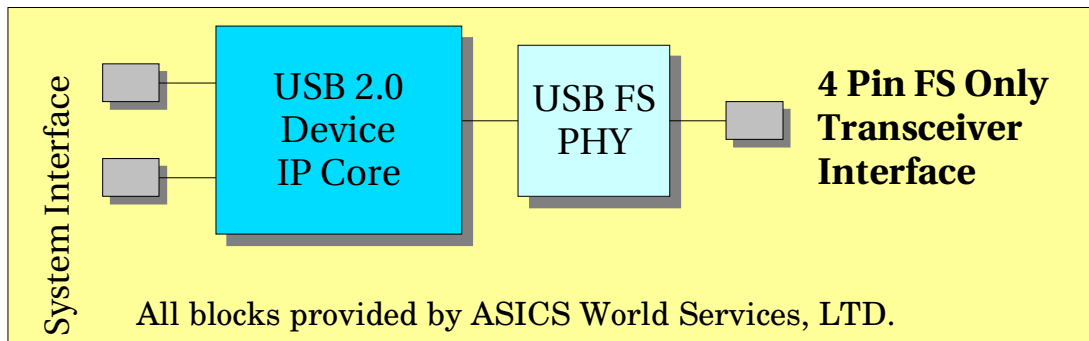
✓AHB ✓OCP ✓OPB ✓PLB ✓AVALON ✓WISHBONE ✓CUSTOM

### System Configuration Examples

1) Default configuration, raw UTMI+ L2 interface



2) FS Only configuration with ASSP USB 2.0 Transceivers



3) ULPI PHY Interface Configuration

