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Product Overview

2.5 Gbps GPON FEC Codec

Introduction

This high performance core is a full featured Forward Error Correction encoder and decoder, specially designed for high speed optical networks or any other broadband applications. It is fully compliant with the 2.5 Gbps GPON standard (G.984.3) and is available for FPGA or ASIC implementation. The FEC algorithm is based on Reed-Solomon (255,239) code and consists of an encoder and decoder module. The encoder module computes 16 parity bytes and appends them on the 239 byte information block. The decoder receives the 255 bytes codeword, locates and corrects up to 8 byte errors being introduced in the transmission channel.

Features

- Fully compliant with the ITU-T G.984 (GPON), ITU-T G.983 (BPON) and ITU-T G.709 recommendations.
- Supports ASIC and FPGA implementation technologies.
- Single edge, fully synchronous design.
- Area efficient design.
- Symbol rate clock.
- Supports both streaming of data and gaps between codeword bytes.
- Calculates the number of erroneous bytes.
- Generates a status signal indicating error locations.
- Determines the location and magnitude of the erroneous bytes.
- Corrects up to 8 erroneous bytes.
- Detects uncorrectable codewords.
- Predictable low decoder latency.

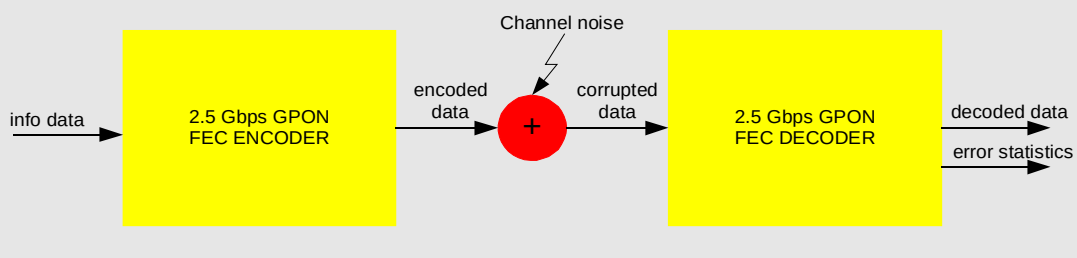
Architecture

The Encoder module receives blocks of 239 information bytes and calculates on the fly 16 parity bytes for each incoming information block. Data can be received continuously or with gaps. Since the encoder is systematic, the 239 information symbols are transmitted unaltered. The parity bytes are appended at the end of the information block to form a 255 bytes codeword. The generator polynomial of the RS (255,239) code is given by:

$$G(x) = (x+1)(x+\alpha)(x+\alpha^2)....(x+\alpha^{15}) ,$$

where α is a root of the primitive polynomial $p(x) = x^8+x^4+x^3+x^2+1$, and is equal to 02_{HEX}.

The Decoder module receives the corrupted channel data, detects the error locations, calculates the error magnitudes and corrects the errors. It can detect and correct up to eight errors introduced in the 255 bytes codeword. If the encountered errors are greater than 8, then the decoder marks the codeword as uncorrectable, asserts the corresponding flag and the information is sent out without correction. Data can be received continuously or with gaps.



Applications

- Gigabit optical access network systems based on ITU-T G.984 recommendation.
- Broadband optical access network systems based on ITU-T G.983 recommendation.
- Optical transport network systems based on ITU-T G.709 recommendation.
- High rate LAN & MAN applications.
- Digital video and audio applications.
- Satellite broadcast.

Size And Speed

The core has been targeted to both ASIC and FPGA technologies for various applications. Specifically, for ASIC implementations, two alternative architectures (AREA or SPEED) are offered. The choice is driven by the data throughput and gate count requirements.

Indicative synthesis results are shown in the following table:

Silicon Vendor	***Device***		***Resources***		***Performance***	
			Encoder	***Decoder***	***Encoder***	***Decoder***
Xilinx	Virtex II		600 CLB Slices	6400 CLB Slices / 6 Block RAMS	3360 Mbps / 140 MHz	2784 Mbps / 116 MHz
TSMC	0.18µm standard cell libraries	AREA	2.5K gates	18K gates / 8K RAM bits	2640 Mbps / 330 MHz	2560 Mbps / 320 MHz
		SPEED	7.5K gates	54K gates / 24K RAM bits	7920 Mbps / 330 MHz	7680 Mbps / 320 MHz

Code Performance

The GPON Reed-Solomon code performance is typically illustrated with a BER vs SNR curve. As shown in the following figure the optical coding gain at 10^{-12} BER is 5.4 dB.