ASICS ws

Product Overview

USB 2.0 On-The-Go IP Core

Introduction

A 'Dual-Role' USB 2.0 *On-The-Go* IP Core that operates as both an USB 2.0 peripheral or as an USB 2.0 OTG host in a point-to-point communications with another USB device.

Features

The USB OTG IP Core is fully USB 2.0 and USB 2.0 *On-The-Go* Supplement compliant. The main features of the USB OTG IP Core are:

- True Dual-Role capability
- OTG high performance host mode
- UTMI+ L2 Interface, ULPI wrapper and FS only transceiver interface available
- Full USB peripheral support
- Session request protocol support
- Host negotiation protocol support
- High, Full and Low Speed mode support
- Up to 16 endpoints
- Bulk, interrupt and isochronous transfers
- Slave and Master System Interface:
  - ✔ AVALON
  - ✔ AHB
  - ✔ OCP
  - ✔ OPB
  - ✔ PLB
  - ✔ WISHBONE
  - ✔ Customer specified bus interface
- No dedicated local memory required
- Compact and cost-effective solution for SoC

An USB OTG IP Core is ideal for applications where the target device must act as a peripheral and as a host, depending the situation. It provides portable devices with a cost-effective way of conducting point-to-point communications using the USB bus.

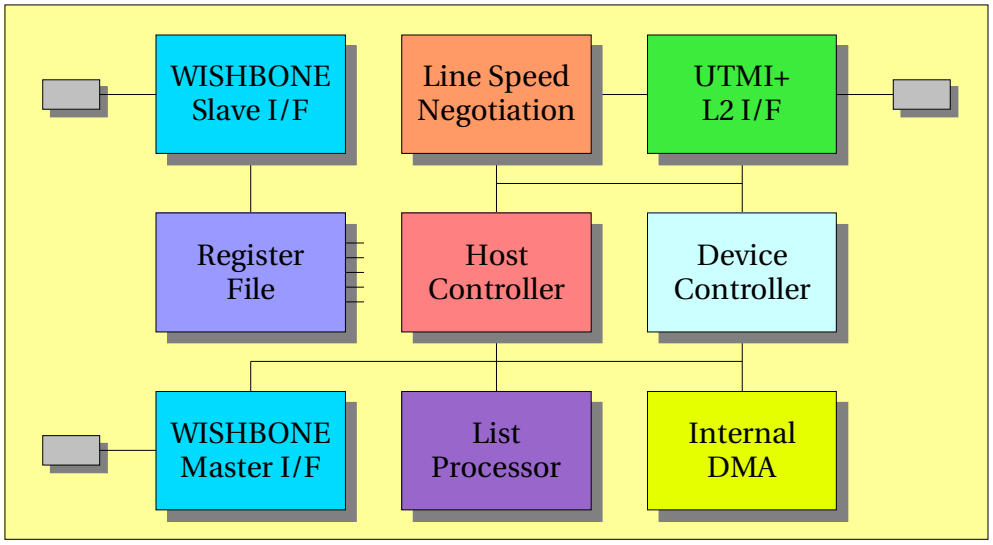
A good example is a PDA which has to be a peripheral that can sync with a host PC, but can also be a host when a peripheral, such as a keyboard or a camera, is connected to it.

Architecture

The USB 2.0 OTG IP Core supports Low Speed, Full Speed and High Speed operations. It will automatically perform the required negotiation to determine if it's counter part supports High Speed and fall back to Full Speed operation if it does not. The speed negotiation is supported in device and host modes.

UTMI+ L2 PHY Interface

The USB 2.0 OTG IP Core features an industry standard UTMI+ L2 interface. Any of-the-shelf UTMI+ L2 compliant PHY or PHY IP can be used with this IP Core.



Architecture (cont.)

MCU Interfaces

The USB 2.0 OTG IP Core features two WISHBONE interfaces, which can be easily adapted to AMBA AHB bus interface with our WISHBONE/AMBA bridge.

The Slave Interface is used to access all core internal registers.

The Master Interface allows the USB 2.0 OTG IP Core to share the system memory for buffering data. It is also used to store Transfer Descriptors when operating in Host Mode.

Buffer Memory

The USB 2.0 OTG IP Core does not need dedicated buffer memory. It's WISHONE Master Interface and the internal DMA engine allow it to share the SoC's main memory for its buffers. Optionally we can also provide a WISHBONE bridge to attach standard dedicated SRAM.

The Host Controller block is active when the USB OTG IP core operates in a OTG host mode. In this mode it can control USB peripherals that are attached to it. It provides full support for session request and host negotiation protocols.

Verification

The USB 2.0 OTG IP Core comes with an elaborate test bench that demonstrates the usage and programing of the USB 2.0 OTG IP Core.

Size And Speed

Sample synthesis results for an implementation with 4 endpoints.

Technology	*Gate Count*	*Operating Frequency*
UMC 0.18u	40K Gates	60MHz PHY, >200MHz WISHBONE
Xilinx Vertex 2 1000 -5	4185 LUTs (40%)	60MHz PHY, >110MHz WISHBONE
Altera Stratix 2 EP2S90 -4	7515 ATOMs (10%)	60MHz PHY, >130 MHz WISHBONE

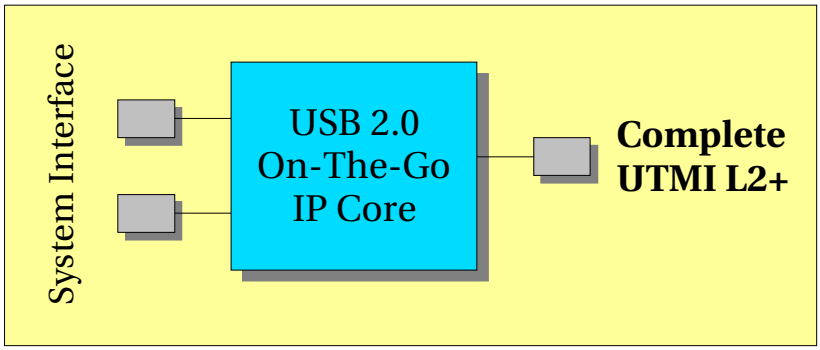
These synthesis results are provided for reference only. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

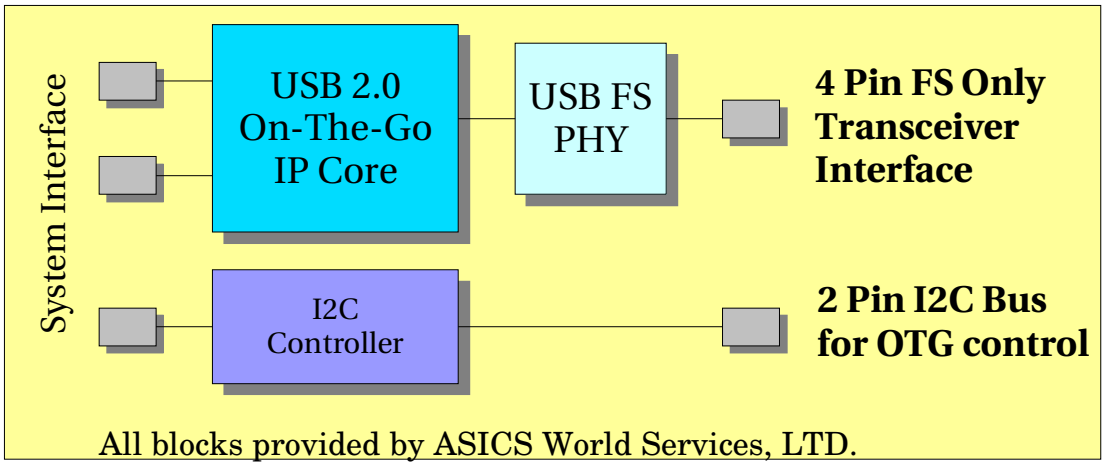
✓AHB ✓OCP ✓OPB ✓PLB ✓AVALON ✓WISHBONE ✓CUSTOM

System Configuration Examples

1) Default configuration, raw UTMI L2+ interface



2) FS Only configuration with ASSP OTG Transceivers



3) ULPI PHY Interface Configuration