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Product Overview

16 Bit RISC DSP IP Core

Introduction

A 16 bit true RISC Architecture Digital Signal Processor for embedded applications that require high performance in a small form factor with ultra low power consumption.

Features

An optimized Harvard Architecture based RISC engine, is the hart of the DSP. Targeted to embedded applications with varying needs, this DSP has it all:

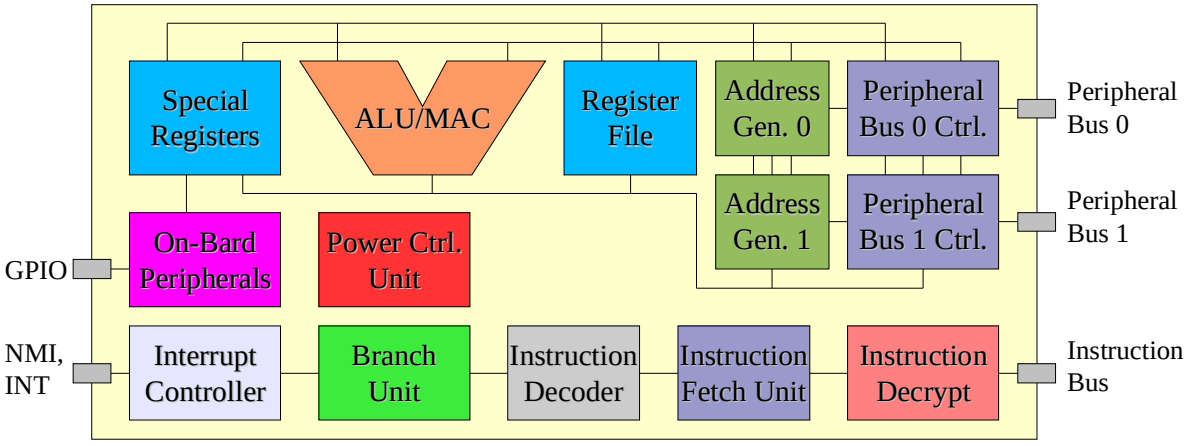
- ✔ Up to 128 General Purpose Registers
- ✔ Windowed Register File (up to 15 windows)
- ✔ Two Address generators with 8 Address and 8 Mask registers each, Circular Buffer support
- ✔ Standard DSP operation such as MUL, MAC, DIVide, REPeat instructions
- ✔ Extensible Instruction Set
- ✔ Separate Instruction and Data buses
- ✔ Two Peripheral Buses
- ✔ Low Power Architecture
- ✔ Variable size Hardware Stack
- ✔ 65 Instructions Default Instruction Set
- ✔ Built in Instruction Decryption
- ✔ 16 Interrupts; 1 NMI; 32 Traps
- ✔ 128 GPIO (optional: UART, PCM, SPI)

The instruction set and the ALU can be easily customized by adding or removing instructions. However the default instruction set should satisfy most customers needs.

By separating the instruction and data buses, it is guaranteed that there will be no contention between instruction fetches and memory/peripheral accesses. Instruction and data path width can also be independently changed.

Dual Peripheral Buses provide for easy filter implementation.

Digitally controlled power management allows the clock to be linearly scaled. A Sleep Mode provides even greater power savings by disabling the clock altogether.



Architecture

A simple architecture with clearly defined structures and buses makes this DSP a very compact solution while keeping the cycle time very short.

The main data path, clearly connect the ALU/MAC with internal registers and the two Peripheral Bus Interfaces. Data can flow to and from the units without any restrictions, providing full utilization of all resources.

Instructions are fetched from the instruction bus and immediately decoded in to various control signals. These control signals select the actual operations and perform data steering.

A variable size hardware stack allows for very fast task switching, and subroutine calling.

Eight global and eight bank switched (window) registers. Up to 15 windows (128 registers) are supported, providing flexible, RAM-less environment.

Two Address Generators provide 8 Address and 8 Mask registers each. Supporting such features like circular buffers and auto increment make implementing filters and other signal processing tasks easy and straight forward.

Instruction encryption provides a fast and effective mechanism to protect proprietary code and intellectual property. More than 68 billion possible combinations make it virtually impossible to reverse engineer the instruction sequence.

One non-maskable interrupt (NMI) and 16 maskable interrupts can be used to monitor external time critical events. 32 Trap levels (up to 64) provide an easy interface to create an API.

A Power Control Block allows for DSP to be slowed down by a factor of 1/1 to 1/512. Practically this is equivalent to dividing the clock by a factor of 1/1 to 1/512. In addition a sleep mode provides zero toggling while waiting for an external interrupt. Accesses to the Peripheral Buses are always performed at full speed, allowing Digital Filter tasks to run at full speed while other operations run at a fractional speed.

Size And Speed

Sample Synthesis results for a RDSP with 16 level HW stack, 7 register windows (64 total registers) and 128 pin GPIO and 4 Address and 4 Mask registers in each Address Generators. The goal was smallest and fastest implementation.

Technology	*Gate Count*	*Fmax*	*MAC/Sec*
Xilinx Virtex II 500	3659 LUTs (59%)	63 MHz	63M
UMC 0.18u (Performance Optimized)	36.6K Gates [1]	220 MHz	220M
UMC 0.18u (Area Optimized)	26.4K Gates [1]	100 MHz	100M

These synthesis results are provided for *reference only*. Please contact us for estimates for your application.

1 Memories not included. Memory size for the register file ranges from 16 to 128 registers of 16 bits each, depending on the number of windows selected. Memory for the Hardware stack can be 2 to 256 entries of 16 bits each. Memories for Address Generators can be 2 to 8 entries each for Address and Mask registers for each DAG.