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Product Overview

16 Bit RISC MCU IP Core

Introduction

A 16 bit true RISC Architecture Microcontroller for embedded applications that require high performance in a small form factor with ultra low power consumption.

Features

An optimized Harvard Architecture based RISC engine, is the hart of the MCU. Targeted to embedded applications with varying needs, this MCU has it all:

- ✔ up to 128 General Purpose Registers
- ✔ Windowed Register File (up to 15 windows)
- ✔ Extensible Instruction Set
- ✔ Separate Instruction and Data buses
- ✔ Low power architecture
- ✔ Variable size Hardware Stack
- ✔ 51 instructions default instruction set
- ✔ Built in instruction decryption
- ✔ 16 Interrupts; 1 NMI; 32 Traps
- ✔ 128 GPIO (optional: UART, I2C, SPI)

The instruction set and the ALU can be easily customized by adding or removing instructions. However the default instruction set should satisfy most customers needs.

By separating the instruction and data buses, it is guaranteed that there will be no contention between instruction fetches and memory/peripheral accesses. Instruction and data path width can also be independently changed.

Digitally controlled power management allows the clock to be linearly scaled. A Sleep Mode provides even greater power savings by disabling the clock altogether.

Architecture

A simple architecture with clearly defined structures and buses makes this MCU a very compact solution while keeping the cycle time very short.

The main data path, clearly connect the ALU with internal registers and an data load/store unit. Data can flow to and from the units without any restrictions, providing full utilization of all resources.

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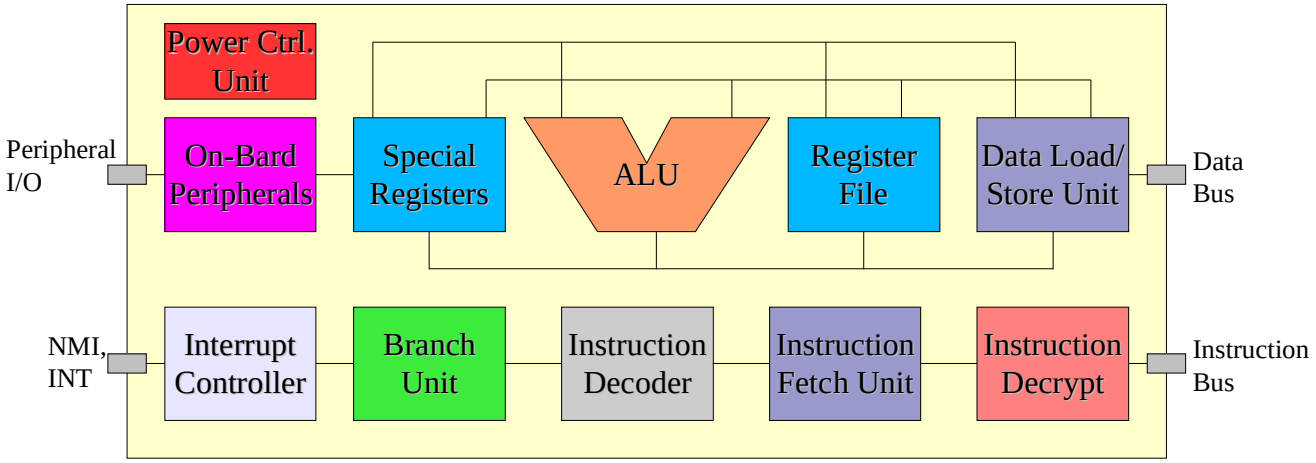

Instructions are fetched from the instruction bus and immediately decoded in to various control signals. These control signals select the actual operations and perform data steering.

A variable size hardware stack allows for very fast task switching, and subroutine calling.

Eight global and eight bank switched (window) registers. Up to 15 windows (128 registers) are supported, providing flexible, RAM-less environment.

Instruction encryption provides a fast and effective mechanism to protect proprietary code and intellectual property. More than 68 billion possible combinations make it virtually impossible to reverse engineer the instruction sequence.

One non-maskable interrupt (NMI) and 16 maskable interrupts can be used to monitor external time critical events. 32 Trap levels (up to 64) provide an easy interface to create an API.

A Power Control Block allows for MCU to be slowed down by a factor of 1/1 to 1/512. Practically this is equivalent to dividing the clock by a factor of 1/1 to 1/512. In addition a sleep mode provides zero toggling while waiting for an external interrupt.

Size And Speed

Sample Synthesis results for a RMCU with 16 level HW stack, 7 register windows (64 total registers) and 128 pin GPIO.

Technology	*Gate Count*	*Fmax*
Xilinx Spartan IIe 100	1850 LUTs (75%)	60 MHz
UMC 0.18u (Area Optimized)	12.4 K Gates [1]	110 MHz
UMC 0.18u (Performance Optimized)	16.2 K Gates [1]	300 MHz

These synthesis results are provided for *reference only*. Please contact us for estimates for your application.

1 Memories not included. Memory size for the register file ranges from 16 to 128 registers of 16 bits each, depending on the number of windows selected. Memory for the Hardware stack can be 2 to 256 entries of 16 bits each.