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Product Overview

Reed Solomon Decoder IP Core

Introduction

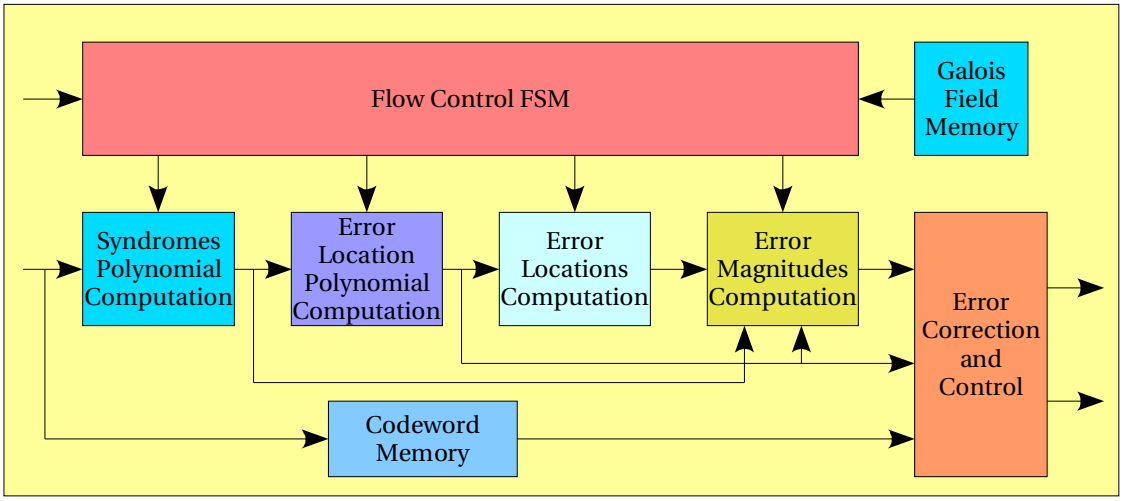
This high performance, fully programmable Reed Solomon Decoder IP Core is intended for use in a wide range of applications requiring forward error correction and can be targeted in any ASIC or FPGA technologies.

In channel coding redundancy is inserted in the transmitted information bit-stream. This redundant information is used in the decoder to eliminate the channel noise. The error correction capability of a FEC system is strongly depended on the amount of redundancy as well as on the coding algorithm itself. The Reed-Solomon decoder receives an N symbol codeword consisting of a K symbol information block appended with 2T parity symbols, locates and corrects up to T possible symbol errors or up to 2T erasure errors anywhere in the codeword. If more than T symbol errors or 2T erasure errors are received then the decoder marks the codeword as uncorrectable.

Features

The main core features features are:

- Continuous, very high-speed, time-domain Reed-Solomon decoding algorithm.
- Supports different Reed-Solomon coding standards.
- Supports error and erasure decoding
- Code rate can be dynamically varied
- Parameterizable bits per symbol (M).
- Programmable codeword length (NVAL) with parameterizable maximum value (N).
- Programmable number of errors (TVAL) with parameterizable maximum value (T).
- Shortened codes supported (NVAL,TVAL).
- User configured primitive field polynomial.
- User configured generator polynomial.
- Predictable decoder latency.



Architecture

The decoder is parameterized in terms of bits per symbol (2^M), maximum codeword length (N) and maximum correction power (T). It also supports shortened codes by varying on the fly the NVAL and TVAL inputs. Therefore any desirable code-rate can be easily achieved rendering the decoder ideal for adaptive FEC applications. If NVAL=2^M-1 then the code is non-shortened. If NVAL is less than 2^M-1 then the code is shortened. The effective code rate is NVAL / (NVAL-2TVAL). The implementation is very low latency, high speed with a simple interface for easy integration in SoC applications.

Application Examples

- Digital Video Broadcast (DVB)
- Digital Satellite Broadcast (ETS 300-421satellite, ETS 300-429 cable)
- Intelsat Earth Stations (IESS-308)
- Space Telemetry Systems (CCSDS)
- ADSL Transceivers (ITU G.992.1)
- Wireless Broadband Systems (IEEE 802.16)
- 2.5G, 10G and 40G Optical Networks (ITU-T G.795)
- Data Storage and Retrieval Systems (e.g. CD-ROM, DVD, Compact Flash)

Customization

This IP can be customized to specific application requirements for optimum area and speed results.

1. Primitive polynomial
   e.g. P(x) = x8+x4+x3+x2+1
2. Generator polynomial
   e.g. G(x)=(x+a0) (x+a1) ...(x+a15)
3. Bits per symbol (M)
4. Message and codeword length
   e.g. RS(255,239
5. Number of parity symbols (2T)
6. Fixed or variable on the fly message length (NVAL)
7. Fixed or variable on the fly error correction capability (TVAL)

Performance

Example configurations showing actual average latency and bandwidth.

Parameter / Mode	*ATSC*	*DVB*	*CCSDS*	*802.16*	*IESS 308*
N	207	204	255	255	255
T	10	8	16	8	10
Latency (average cycles)	504	462	630	495	516
Bandwidth (average clock cycles per symbol)	1.22	1.13	1.24	1.01	1.01
Bandwidth @100 MHz[1]	655	707	645	792	792

1 In Mbps for M=8

Size And Speed

The decoder can be easily customized for specific area or speed requirements. The area is heavily depended on the maximum error correction capability.

Sample synthesis results for the variable on-the-fly code rate version of Reed Solomon Decoder IP core, with N=255 and T=8 for a (255,239) code, are shown in the following table. The goal was smallest and fastest implementation.

Technology	*Gate Count*	*Fmax*
Xilinx Spartan 3e (xc3s1200e-5)	3005 Slices	> 80 MHz
Xilinx Virtex 4 (4vlx25-11)	3345 Slices	> 125 MHz
Xilinx Virtex 5 (xc5vlx30-1)	1460 Slices	> 150 MHz
UMC 0.13u	12K Gates	> 200 MHz

These synthesis results are provided for *reference only*. Please contact us for estimates for your application.