Reed Solomon Encoder IP Core

Introduction

This high performance, fully configurable Reed Solomon Encoder IP Core is intended for use in a wide range of applications requiring forward error correction and can be targeted in any ASIC or FPGA technologies. In channel coding redundancy is inserted in the transmitted information bit-stream. This redundant information is used for channel noise elimination. The error correction capability of a FEC system is strongly depended on the amount of redundancy as well as on the coding algorithm itself. The Reed-Solomon encoder accepts a K symbol information block and outputs the information block unaltered appended with 2T parity symbols, thus forming an N symbol codeword, where N=K+2T.

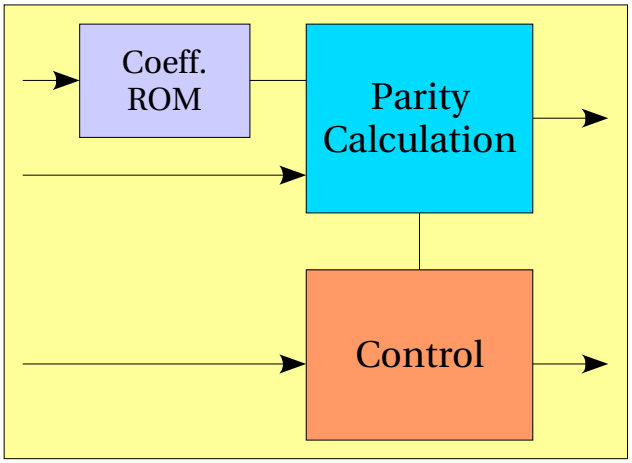
Features

The main core features features are:

- Supports many different Reed-Solomon coding standards
- Code rate can be dynamically varied
- Parameterizable bits per symbol (M)
- Programmable codeword length (NVAL) with parameterizable maximum value (N)
- Programmable number of errors (TVAL) with parameterizable maximum value (T)
- Shortened codes supported (NVAL,TVAL)
- User configured primitive field polynomial
- User configured generator polynomial
- Synchronous design
- Low latency — 2 cycles

Architecture

The encoder is parameterized in terms of bits per symbol (M), maximum codeword length (N) and maximum correction power (T). It also supports shortened codes by varying on the fly the NVAL and TVAL inputs. Therefore any desirable code-rate can be easily achieved rendering the encoder ideal for adaptive FEC applications. If NVAL=2^M-1 then the code is non-shortened. If NVAL is less than 2^M-1 then the code is shortened. The effective code rate is NVAL / (NVAL-2TVAL). The implementation is very low latency, high speed with a simple interface for easy integration in SoC applications.



APPLICATIONS

- Digital Video Broadcast (DVB)
- Digital Satellite Broadcast (ETS 300-421satellite, ETS 300-429 cable)
- Intelsat Earth Stations (IESS-308)
- Space Telemetry Systems (CCSDS)
- ADSL Transceivers (ITU G.992.1)
- Wireless Broadband Systems (IEEE 802.16)
- 2.5G, 10G and 40G Optical Networks (ITU-T G.795)
- Data Storage and Retrieval Systems (e.g. CD-ROM, DVD, Compact Flash)

CUSTOMIZATION

The IP can be customized to specific application requirements for optimum area and speed results. The following implementation parameters need to be specified:

1. Primitive polynomial
   e.g. $P(x) = x^8+x^4+x^3+x^2+1$
2. Generator polynomial
   e.g. $G(x)=(x+a^0)\ (x+a^1)\ldots\ (x+a^{15})$
3. Bits per symbol (M)
4. Message and codeword length
   e.g. RS(255,239)
5. Number of parity symbols (2T)
6. Fixed or variable on the fly message length (NVAL)
7. Fixed or variable on the fly error correction capability (TVAL)

SIZE AND SPEED

The encoder can be easily customized for specific area or speed requirements. The area is heavily depended on the maximum error correction capability.

Sample Synthesis results for Reed Solomon Encoder IP Core, with N=255 and T=8 for a (255,239) code. The goal was smallest and fastest implementation.

Technology	***Gate Count***	***Fmax***	***Throughput (@Fmax)***
Xilinx Spartan 3e (xc3s1200e-5)	1106 Slices	> 110 MHz	880 Mbps
Xilinx Virtex 4 (4vlx25-11)	989 Slices	>180 MHz	1.44 GBps
Xilinx Virtex 5 (xc5vlx30-1)	306 Slices	>200 MHz	1.6 GBps
UMC 0.13u	5.4K Gates	>300 MHz	2.4 Gbps

These synthesis results are provided for *reference only*. Please contact us for estimates for your application.