ASICS.ws

Product Overview

Serial Attached SCSI (SAS) Initiator IP Core

Introduction

The SAS Initiator Controller IP Core provides an interface to high-speed serial link replacements for the parallel SCSI attachment of mass storage devices. Maximum supported bandwidth is 48 Gbps. The serial link employs multiple high-speed gigabit transceivers.

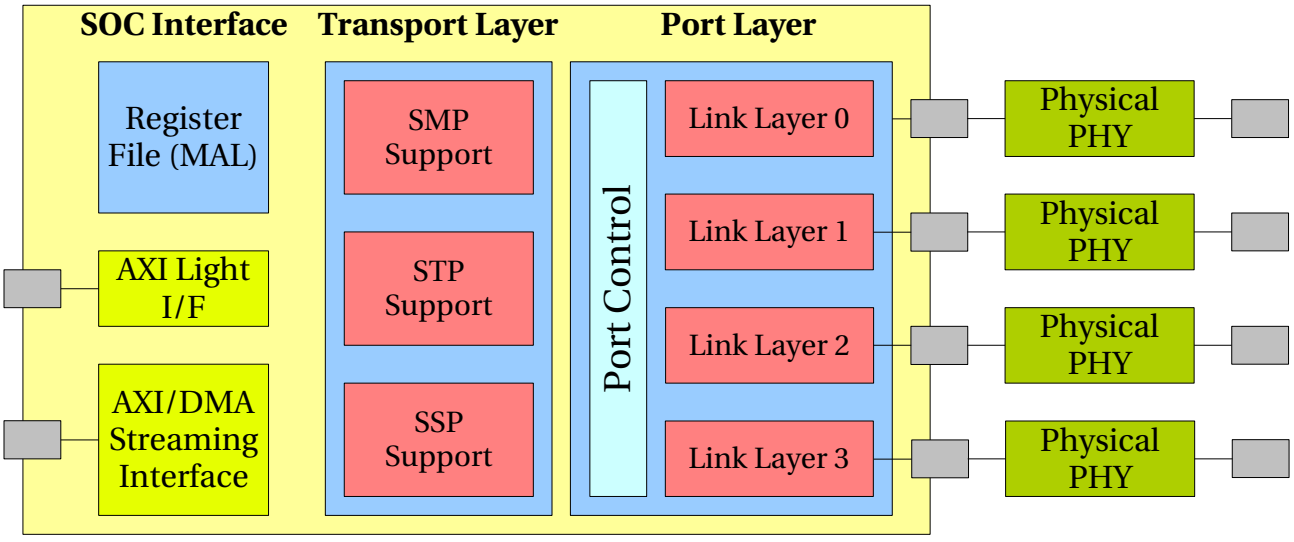
Features

The SAS Initiator IP Core includes the following features:

- *SAS & SATA Speed Negotiation and OOB*
- *SATA 1.5, 3.0 and 6.0 Gbps support*
- *SAS 1.5, 3.0, 6.0 and 12.0 Gbps support*
- *Native 32 bit PHY interface*
- *Rate Tolerance Management*
- *Data and Idle scrambling*
- *Frame assembly and decoding*
- *Power Management*
- *Configurable, 1 quad, 2 dual or 4 single narrow, or 1 quad or 2 dual wide ports*
- *Automatic Identify and Reset Management*
- *Automatic Connection Control*
- *Support of SMP, SSP, SATA protocols*
- *Multi-channel S/G DMA support with on-demand processing*
- *256 bit DATA stream*
- *Multiple simultaneous connections per device*
- *Sustained 48 GBps bandwidth*
- *Up to 32 internal transmit buffers*
- *Up to 32 internal receive buffers*
- *Xilinx Transceiver based PHY*

Architecture

This high performance implementation of a SAS Initiator support every mandated feature outlined by the latest SAS Specification. The implementation is highly configurable,



to provide the most flexibility and satisfy every need.

The design is cleanly partitioned in to the fundamental function blocks of a SAS Initiator:

- PHY (SERDES)
- PHY Layer
- Port Layer
- Link Layer
  - SSP
  - SMP
  - SATA
- Transport Layer
- AXI Interface

We include a FPGA based PHY, or the IP Core can interface to a standard SAS PHY from a 3rd party. The FPGA based PHY is targeted for Xilinx series 7 devices, with GTX and GTH transceivers. Our PHY includes all functions required to bring up the link all the way to 12G.

The SoC interface consists of a AXI Light interface to access internal registers, and a AXI 4.0 Streaming interface for data transfers.

We have successfully tested this IP Core with the following SAS SSDs:

- HGST 200GB SAS-12G SSD
- Seagate 200GB SAS-12G SSD
- Toshiba 200GB SAS-12G SSD
- Micron 100GB SAS-6G SSD
- Talos (OCZ) 200GB SAS-6G SSD

Size And Speed

Sample Synthesis results for SAS Initiator IP Core. The goal was smallest and fastest implementation.

Technology	*Gate Count*	*Fmax*
Xilinx Virtex 7 GTX/GTH	22K LUTs, 64 BRAMs	175 MHz

These synthesis results are provided for reference only. Shown is a typical implementation with two ports.