Serial ATA I/II Device Controller IP Core

Introduction

The Serial ATA Device Controller IP Core provides an interface to high-speed serial link replacements for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes Gigabit technology and 8b/10b encoding.

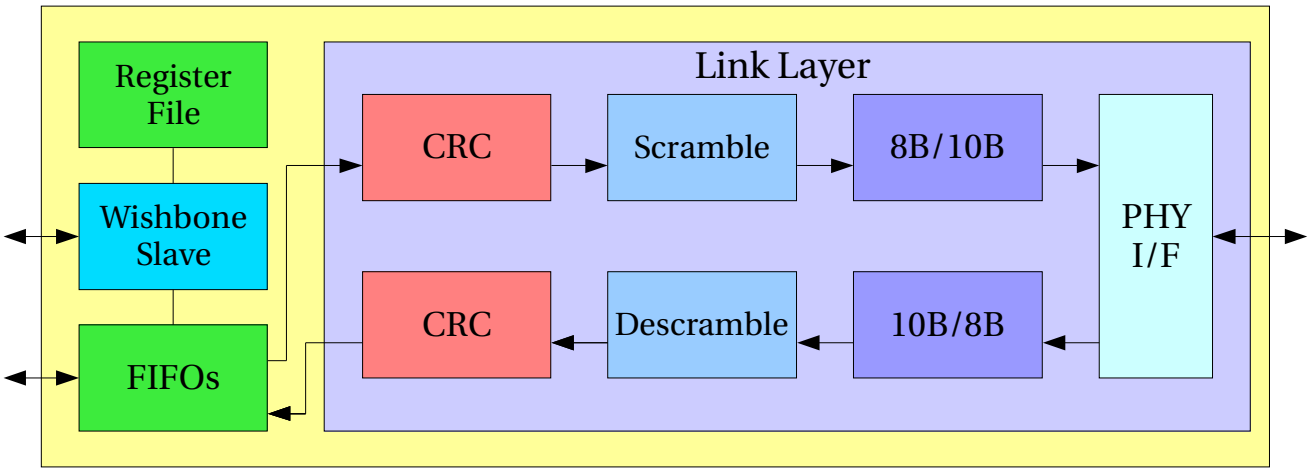
Features

This core is fully compliant to the Serial ATA 1.0a specification and provides some features of the Serial ATA II extensions. The main features are:

- 10 bit Phy interface
- Connects to SAPIS compliant serial ATA Phy
- Fully compliant to SATA Gen 1(1.2 Gb/s) and Gen 2 (2.4 Gb/s)
- Wishbone slave interface for register access and FIFO/DMA data transfers
- Only very few FF's in the Phy clock domain, main part on the Wishbone clock
- 128 byte (32 double word) data FIFO (optional 256 byte)
- Parallel ATA legacy software compatibility
- Implements the Task File, the non-standard serial ATA status and control registers, specific device registers and native mode registers
- interrupt and DMA handshake (external DMA)
- 48-bit address feature set supported
- 8b/10b coding and decoding
- CONT and data scramblers to reduce EMI
- CRC generation and checking
- Auto inserted HOLD primitives
- Power management support (partial and slumber)
- Optional native mode programming model
- Many configuration options

Architecture

The Serial ATA Link and Transport Layer Core implements a serial ATA device interface which connects to a SATA PHY via a 10bit interface and



provides a WISHBONE slave interface for register and DMA access. It consists of the link layer module - with 10bit data paths to the physical layer - and a transport layer module which connects to the system via a WISHBONE slave interface.

SAPIS PHY Interface

This interface connects to any SAPIS compliant serial ATA PHY. Power management and speed negotiation signals are included. The PHY interface is synchronous to the PHY clock domain, which may have a different clock frequency than the system clock domain. Synchronization is done by the Serial ATA Link and Transport Layer Core.

Wishbone Slave Interface

The slave interface is used to access all core internal registers as well as the data FIFO. Software or an external DMA unit can write transmit data into the data FIFO or can read from the FIFO.

DMA Handshake

Simple handshake signals are provided to connect a DMA unit to the core module. The DMA requests will be asserted as soon as any transmit data is available or is needed in the core's data FIFO. The DMA unit will then access the data FIFO via the WISHBONE slave interface. A system interrupt will inform device software on completion of a data transfer.

Automatic flow control mechanisms control data throttling to avoid underflow or overflow of the transmit data FIFO. The DMA unit (or device software) may work at any speed without the risk of data loss. Data FIFO thresholds can be adjusted to optimize the data flow control.

Size And Speed

Sample Synthesis results for SATA Device IP Core. The goal was smallest and fastest implementation.

Technology	*Gate Count*	*Fmax*
UMC 0.18u	23.5 K Gates	up to 300MHz PHY clock up to 200 MHz SoC clock
Xilinx Virtex 4 (XC4VFX20-10)	1794 Slices	150MHz PHY clock > 110 MHz SoC clock
Xilinx Virtex 5 (XC5VLX50T-2)	1057 Slices	150MHz PHY clock > 125 MHz SoC clock

These synthesis results are provided for *reference only*. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

✓AHB ✓OCP ✓OPB ✓AVALON ✓WISHBONE ✓CUSTOM