

### Serial ATA I/II/III Host Controller IP Core

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#### INTRODUCTION

The Serial ATA Host Controller IP Core provides an interface to high-speed serial link replacements for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes Gigabit technology and 8b/10b encoding.

#### FEATURES

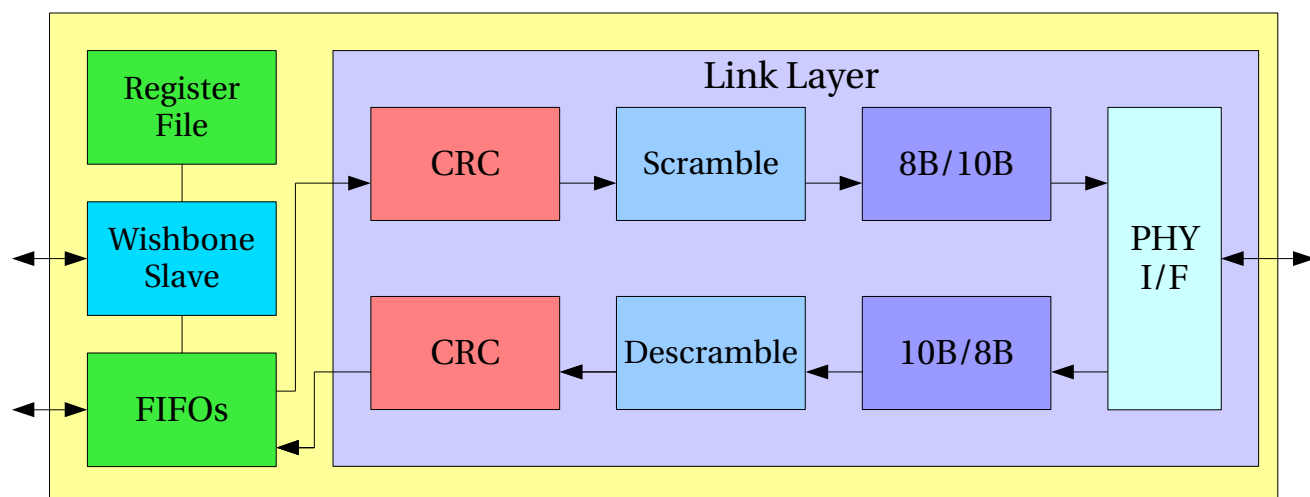
This core is fully compliant to the Serial ATA 3.0 specification. The main features are:

- High Throughput: **531** MBytes/sec Read, **505** MBytes/sec Write
- Low Latency: **66K** IOPS Read, **67K** IOPS Write (4k blocks)
- Asynchronous, unrestricted SoC clock, independent of PHY clock
- Includes Xilinx Transceiver based PHY
- Fully compliant to SATA V3.0
  - NCQ
  - FIS based switching
- Supports 1.5 Gbps, 3.0 Gbps and 6.0 Gbps

- **AXI Light** interface for register access
- **AXI Stream** Interface and for data transfers
- Full support for PIO, DMA and FPDMA transfers
- Implements the shadow register block and the serial ATA status and control registers
- Parallel ATA legacy software compatibility
- 48-bit address feature set supported
- Power management support (partial and slumber)
- DMA Support
  - Descriptor Based Command Processing
  - Unlimited command list size
- Many configuration options
- ucLinux Drivers

#### ARCHITECTURE

The Serial ATA Link and Transport Layer Core implements a serial ATA host interface which connects to a SATA PHY via a 10/20/40 bit interface and provides a Wishbone slave interface for register and DMA access.



It consists of the link layer module - with 10/20/40 bit data paths to the physical layer - and a transport layer module which connects to the system via a Wishbone slave interface.

### SAPIS PHY INTERFACE

This interface connects to any SAPIS compliant serial ATA PHY. Power management and speed negotiation signals are included. The PHY interface is synchronous to the PHY clock domain, which may have a different clock frequency than the system clock domain. Synchronization is done by the Serial ATA Link and Transport Layer Core.

### DMA HANDSHAKE

Simple handshake signals are provided to connect a DMA unit to the core module. The DMA requests will be asserted as soon as any transmit data is available or is needed in the core's data FIFO. The DMA unit will

then access the data FIFO via the Wishbone slave interface. A system interrupt will inform host software on completion of a data transfer.

Automatic flow control mechanisms control data throttling to avoid underflow or overflow of the transmit data FIFO. The DMA unit (or host software) may work at any speed without the risk of data loss. Data FIFO thresholds can be adjusted to optimize the data flow control.

### SIZE AND SPEED

Sample Synthesis results for SATA Host IP Core. The goal was smallest and fastest implementation.

<i>Technology</i>	<i>Gate Count</i>	<i>Fmax</i>
UMC 0.18u	24K Gates	>200 MHz SoC clock
Xilinx Virtex 5 (XC5VLX50T-2)	1169 Slices	>135 MHz SoC clock
Xilinx Virtex 6 (XC6VLX240T-1)	834 Slices	>135 MHz SoC clock
Xilinx Spartan 6 (XC5VFX70T-1)	880 Slices	>100 MHz SoC clock
Kintex 7 (XC7K325T-1)	758 Slices	>180 MHz SoC clock
Stratix IV (EP4SGX230KF40C2)	2581 LC Comb.	>180 MHz SoC clock

These synthesis results are provided for reference only. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

✓AXI ✓AHB ✓OCP ✓OPB ✓AVALON ✓WISHBONE ✓CUSTOM