

SATA Port Multiplier IP Core

INTRODUCTION

A Port Multiplier connects one Serial ATA host bus adapter to multiple Serial ATA devices. Only one active host connection to the Port Multiplier is supported. This implementation provides one top level module for every number of devices from 2 to 15.

FEATURES

The core is compliant to the Serial ATA International Organization: Port Multiplier (Revision 1.2, 27-January-2005). The main features are

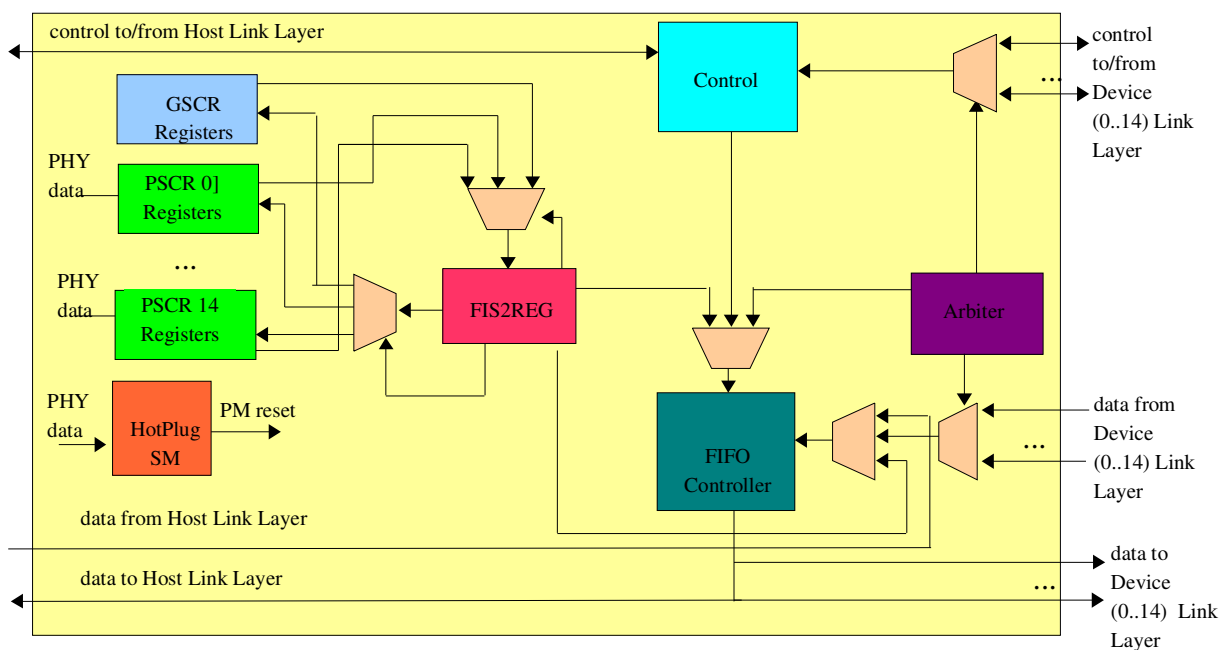
- supports maximum fan-out of 15 device connections
- 128 byte (32 double word) data FIFO (optional 256 byte)
- Hot plug support
- Supports booting with legacy software on device port 0h
- Supports mandatory General Status and Control Registers

- Supports Port Status and Control Registers for each supported device port
- Many configuration options
- Compact and cost-effective solution

ARCHITECTURE

The basic representation of the internal structure of the Port Multiplier implementation is shown below.

The Serial ATA Port Multiplier implements hot plug state machines (HotPlugSM) as defined by the SATA Port Multiplier Specification (Revision 1.2). The reset behavior has been implemented according to this document. The arbitration (Arbiter) between multiple devices sending a transmit request at the same time is done by a simple round robin arbiter which checks one device every clock cycle. When a device with an active request is found, then the round robin is stopped until the request is accepted or withdrawn. The helper module (FIS2REG) latches information trickling out of the data FIFO after a successful RH2D FIS from the host controller to the control port of the port multiplier. From this data the signals required to access the register blocks are created.



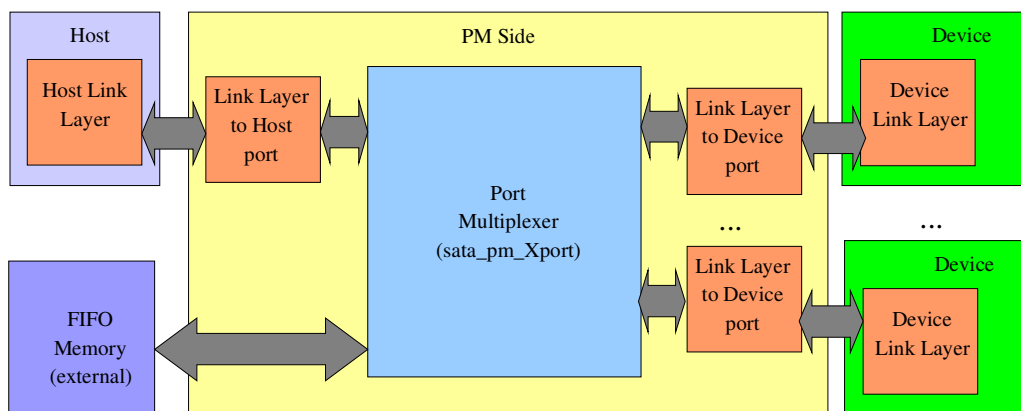
ARCHITECTURE (CONT.)

In addition it controls the data flow back from the register blocks to the data FIFO. FIFO controller controls access to the external memory. The central controller for the Serial ATA Port Multiplier Core IP (Control) is responsible for controlling transmissions from Host to Device, from Device to Host and from Host to PM. It is also responsible for detecting collisions when the Port Multiplier has already started a reception from the device that the host wants to transmit to. GSCR module implements Global Status and Control Registers of a Serial ATA Port Multiplier according to the specification. PSCR module implements Port Status and Control

Registers of a Serial ATA Port Multiplier according to the specification. This module is instantiated once for every device port of the Serial ATA Port Multiplier. The Port Multiplier registers are accessed using Read/Write Port Multiplier commands issued to the control port.

IMPLEMENTATION

The PM core is connected to the Host controller and to the devices it supports through a Link layer for each connection. The link layer is responsible for transmitting and receiving a data stream which gets intermixed with control primitives. The data will be scrambled, a CRC will be added or checked, and 8b/10b encoding and decoding is performed.



SIZE AND SPEED

Sample synthesis results for an implementation with 4 ports.

Technology	Number of Ports	Gate Count	Operating Frequency
Xilinx Virtex 5 (xc5vlx50t)	4	2933 Slices	150 MHz
Xilinx Virtex 5 (xc5vlx50t)	8	4687 Slices	150 MHz
UMC 0.18	4	62K Gates	150 MHz
UMC 0.18	8	110K Gates	150 MHz

These synthesis results are provided for reference only. Please contact us for estimates for your application.