ASICS ws

Product Overview

SPI Flash Controller

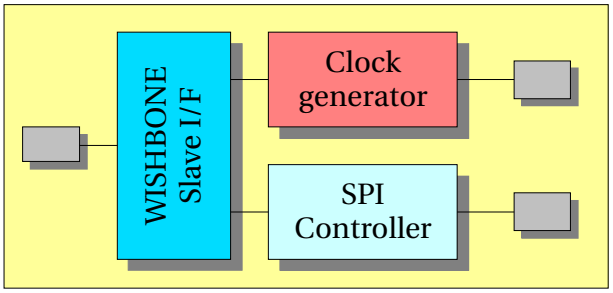
Introduction

The SPI FLASH controller provides an simple interface to serial FLASH devices, which are memory mapped in to the SoC memory space.

Features

The SPI FLASH interface IP core is an easy to use building block that provides the following features:

- Supports up to 8 FLASH Devices on a single SPI bus
- Supports FLASH devices up to 16MBytes each
- Flash is directly memory mapped in to the SoC memory space
- Supports high speed FLASH devices, up to 50 Mhz
- Can directly boot from FLASH after power on
- Software assistant FLASH programming
- SoC Interface:
  - ✔ AVALON
  - ✔ AHB
  - ✔ OCP
  - ✔ OPB
  - ✔ PLB
  - ✔ WISHBONE
  - ✔ Customer specified bus interface
- No dedicated local memory required
- Compact and cost-effective solution for embedded applications



Size And Speed

Technology	*Gate Count*	*Operating Frequency*
UMC 0.18u	6.6K Gates	50MHz SPI, >250MHz WISHBONE
Xilinx Vertex 2 1000 -5	3000 LUTs	50MHz SPI, >140MHz WISHBONE

These synthesis results are provided for reference only. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

✓AHB ✓OCP ✓OPB ✓PLB ✓AVALON ✓WISHBONE ✓CUSTOM