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Product Overview

USB 3.0 Device IP Core

Introduction

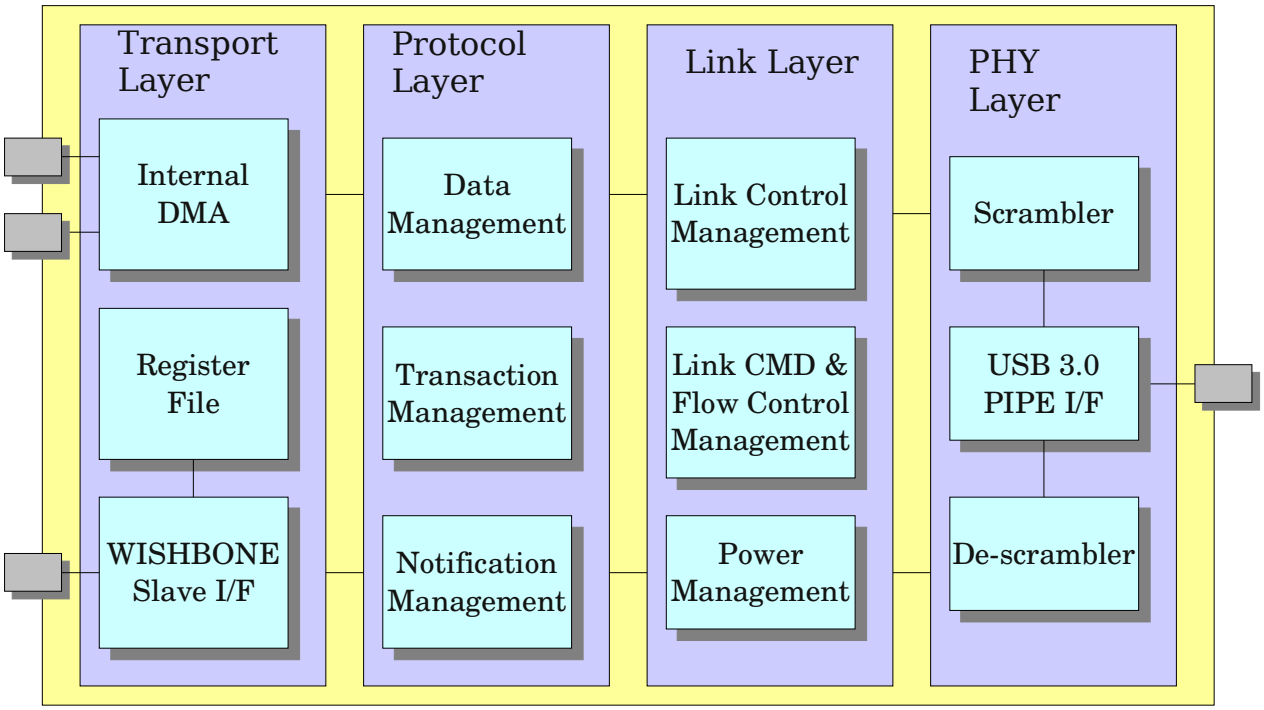
A USB 3.0 Device IP Core that provides high performance SuperSpeed USB connectivity in a small footprint solution for quick and easy implementation of a USB Device interface.

Features

The USB 3.0 Device IP Core is fully USB 3.0 compliant. The main features of the USB 3.0 Device IP Core are:

- USB 3.0 SuperSpeed support, 5Gbit/s
- USB 3.0 PIPE interface (and V5/V6 GTX)
- Integrated DMA engine
- Up to 16 fully configurable endpoints
- Bulk, control, interrupt and isochronous endpoints and transfers
- Automatic Link Control and Management performed in hardware
- User transparent error recovery and re-transmission of packets
- Automatic Power State transition performed in hardware (all power states supported)
- Autonomous operation with very little firmware interaction
- Full duplex operation support
- System Interface:
  - ✔ AHB
  - ✔ AVALON
  - ✔ OCP
  - ✔ OPB
  - ✔ PLB
  - ✔ WISHBONE
  - ✔ Customer specified bus interface
- Compact and cost-effective solution

An USB 3.0 Device IP Core is ideal for applications where the target device must act as a peripheral. It provides portable devices with a cost-effective way of conducting high speed point-to-point transfers using the USB bus.



Architecture (cont.)

The USB 3.0 Device IP Core, implements all required functions to transport USB 3.0 traffic.

This includes the PHY Layer, which implements support functions required to talk to a USB 3.0 PIPE complaint PHY interface; The Link and Protocol layers that implement the USB 3.0 link management, transaction management and data transfers; and the Transport Layer, which provides and interface to external interfaces.

Verification

The USB 3.0 Device IP Core comes with an elaborate test bench that demonstrates the usage and programming of the USB 3.0 Device IP Core.

A reference design is included with each IP Core license. The reference design illustrates how to implement a Mass Storage Device.

Size And Speed

Sample synthesis results for a typical implementation with 4 endpoints.

Technology	*Gate Count*	*Operating Frequency*
Virtex 5 (xc5vfx70t)	3025 Slices	>125 MHz
Virtex 6 (xc6vlx75t)	1661 Slices	>125 MHz

These synthesis results are provided for reference only. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

✓AHB ✓OCP ✓OPB ✓PLB ✓AVALON ✓WISHBONE ✓CUSTOM