ASICS.ws

Product Overview

ZLIB IP Core

Introduction

This is a high performance, small footprint ZLIB compatible IP Core. It features 3 DMA engines, AXI interconnect and separate clocks for AXI interfaces and compression/decompression engines.

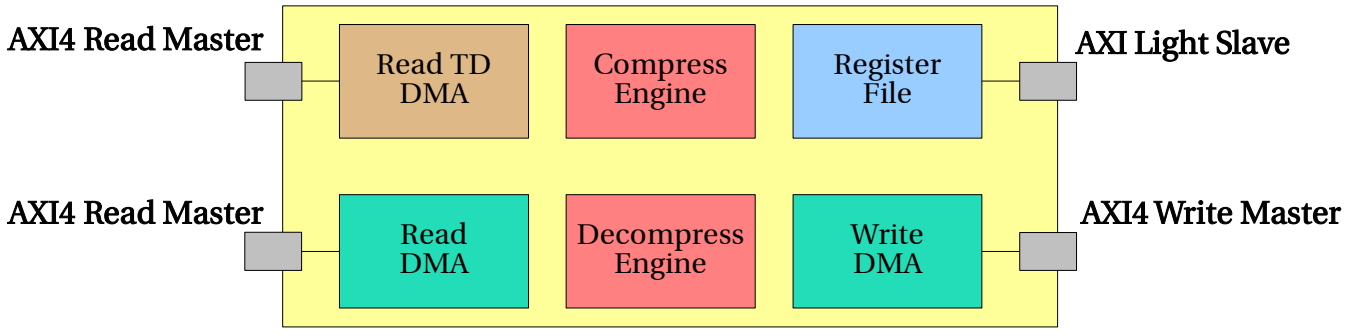
Features

The ZLIB IP Core includes the following features:

- *100% ZLIB compatible*
- *Fixed Huffman encoding*
- *Subset of LZ77*
- *Scatter/Gather DMA engine*
- *Utilizes linked list of transfer descriptors*
- *Compression and Decompression in one IP Core*
- *Configurable Data Path to 32, 64 or 128 bit*
- *Fully AXI-4 compatible*
- *AXI-Light for register Interface*
- *Separate clocks for engines and AXI interface*

Architecture

Separate DMA engines for Scatter/Gather descriptors and data movement, alow non stop processing of data.



Size And Speed

Sample Synthesis results for ZLIB IP Core. The goal was smallest and fastest implementation.

Technology	*Gate Count*	*Fmax*
Virtex UltraScale+ Virtex UltraScale Kintex 7, Virtes 7	2400 CLB LUTs, 3000 Registers, 6 BRAMs	AXI Interface: >200 MHz Engines: >300 MHz
This IP Core can be implemented in any technology. There are no special/dedicated FPGA (or other) components in this IP Core.		

These synthesis results are provided for reference only.